REMARKS

Reconsideration of the application is respectfully requested.

The Office Action at page 2 indicates that the Abstract is not in the proper format. In response, a new Abstract is submitted here that is in proper form.

Regarding the objections to the claims as not having consistent language throughout, most, if not all, of the suggestions given on pages 3 and 4 of the Office Action have been taken and are reflected in claims 1, 3, 14, 22, 25, and 30. Claim 24 has been canceled to obviate the issue of whether or not it limits its base claim 23. A grammatical correction has also been made to claim 23. A typographical error has also been corrected in claim 25. Applicants submit that all of the claim amendments merely make the claim language clearer, and do not alter the scope of the original claim language, which is reasonably clear.

Turning now to the art rejections, claims 1-30 stand rejected as being anticipated by U.S. Patent No. 6,026,016 issued to Gafken ("Gafken"). Applicants respectfully disagree with the rejection for the following reasons.

Beginning with claim 1, a system is recited in which a non-volatile data storage device is configured as one or more storage regions. A program store communicatively coupled to the non-volatile data storage device is to store processor readable instructions to ascertain the validity of data stored in the non-volatile storage device, and, if invalid, to replace the data with an earlier stored valid image of the data. A processing unit that is coupled to the non-volatile data storage device and the program store is to read and process the instructions in the program store. For example, the data in the non-volatile data storage device may be a BIOS, where a processor executes code in the program store to check whether the BIOS found in one or more regions of the non-volatile data storage device has been altered or modified. Gafken does not teach or suggest such a system.

Gafken refers to the difficulty in updating the code in non-volatile memory, where boot code in flash memory has been permanently locked, thereby requiring

physical access (*e.g.*, moving jumpers) in order to reprogram the memory. Gafken proposes a volatile protection bit that is coupled to a non-volatile block in the memory. This bit is programmable, to prevent a memory access operation that is directed to the block. However, Gafken does not teach or suggest a system in which *a processing unit coupled to non-volatile data storage device and program store, reads and processes instructions in the program store to ascertain the validity of data stored in the non-volatile storage device and if invalid to replace the data with an earlier stored valid image of the data.*

According to the Office Action, beginning at page 4, Gafken has a flash memory 115 that is allegedly configured as one or more storage regions (memory array 130). In addition, other memories 125 is indicated as being communicatively coupled to the flash memory 130. However, even assuming such a mapping between Gafken and Applicants' claim 1, Gafken still does not teach or suggest Applicants' system. For example, the Office Action refers to Gafken, at Col. 13, Lines 59-63 as allegedly disclosing Applicants' claimed *program store to store processor readable instructions to ascertain the validity of data stored in the non-volatile storage device and if invalid to replace the data with an earlier stored valid image of the data.* This is incorrect. Gafken states:

> At step 550, it is determined whether a code update has been requested. For one embodiment, this step is performed by reading the operation register 301 to determine whether a code update request is stored in the operation register. If so, then at step 555, **the base address of the code image is read from the base address register 302 to determine where the update image is located in the main memory 125.** [Emphasis added] (Gafken, Col. 13, Lines 52-58)

> That passage in Gafken refers to the capability of the system to obtain the update image from main memory 125. There is no attempt at ascertaining the validity of data that is stored in memory array 130.

> Continuing with Gafken:

> At step 560, any additional code validation is performed and at step 565, the code is updated. The code may be updated by re-programming the entire memory array 130 or by re-programming only desired locations in the memory array 130. (Gafken, Col. 13, Lines 59-63)

That portion of Gafken, however, refers to validating the code (if desired) that will be replacing the code that is currently in the memory array 130. In other words, Gafken only indicates that the code in the memory is to be updated, without teaching or suggesting that the validity of that code be ascertained (and if invalid replaced with an earlier stored valid image). In other words, Gafken is directed only to the updating of the code, but does not describe the need to or the actions of ascertaining the validity of the code that is in the memory array 130.

Accordingly, for the above reasons, the rejection of claim 1 as being anticipated by Gafken is improper and should be withdrawn. Moreover, there is no teaching or suggestion to modify the Gafken technique, so as to read the current content stored in a non-volatile storage device, determine if the current content has been modified without authorization, and replace the current content with a previously stored valid image if the current content has been modified without authorization (see also claim 10).

The Office Action at page 6 refers to Gafken, Fig. 5 and operations 505, 510, 550, and 580 as allegedly disclosing Applicants' claim 10. However, Fig. 5 only discloses a BIOS update procedure without fairly teaching or suggesting that *the current contents stored in a non-volatile storage device be read, a determination made if the current content has been modified without authorization, and the current content being replaced with a previously stored valid image of the content if the current content is determined to have been made without authorization.* Gafken merely describes at step 505 that the code image be retrieved and validated, before updating the flash memory with that image. Step 510 which is described as "request and schedule code update" does not fairly teach or suggest to one of ordinary skill in the art the claimed *reading and determining* operations recited in Applicants' claim 10. Accordingly, reconsideration and withdrawal of the rejection of claim 10 is also requested.}

As to claim 17, Gafken does not teach or suggest a method in which *a non-volatile storage device is arranged into one or more storage regions, an integrity metric corresponding to valid content stored in a first region of the device is generated, and the integrity metric is stored to later determine if the content in the first region has been modified without authorization.*

The Office Action refers to Col. 12 of Gafken as allegedly teaching such a method. However, Gafken describes a flash memory in which a reset detector responds to a control signal on a discrete pin, where this is a write protect or other control signal to be asserted to access the content of flash memory. This is a hardware approach that does not teach or suggest *arranging a non-volatile storage device into one or more regions and generating an integrity metric corresponding to valid contents stored in a first region of the device, and storing the integrity metric to later determine if the content in the first region has been modified without authorization.* Gafken only states that "it may be desirable under certain circumstances to be able to update or make changes to code stored in write protected blocks of a memory array." There is, however, no teaching or suggestion to practice Applicants' claim 17 as highlighted above.

As to independent claim 26, this claim recites a machine-readable medium with instructions that when executed by a processor cause operations with limitations similar to those mentioned above in connection with claim 10. Accordingly, claim 26 is not anticipated or obvious for at least the same reasons.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper in view of the relied upon art reference, and to correct obvious errors in the claims, without altering their scope. A Notice of Allowance referring to claims 1-23, and 25-30, as amended here, is therefore requested to be issued at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No.

02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: September 15, 2005

By _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on September 15, 2005.

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Margaux Rodriguez *September 15, 2005*